IN THE CLAIMS:

Claims 1, 8, 14, 15, 21, 28, 34, and 35 have been amended herein. All of the pending claims 1 through 40 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently Amended) A method for hardening at least a portion of a gate oxide layer on a substrate, the method comprising:
supplying a substrate having an oxide layer over at least a portion of the substrate;
forming a resist over at least a portion of the oxide layer;
patterning the resist to create at least one exposed area of the oxide layer;
hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment having a temperature approximately less than 90°C;
forming a second resist over at least a portion of the oxide layer;
patterning the second resist to create at least one exposed area of the oxide layer; and
conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one nonhardened area within the oxide layer.

2. (Original) The method of claim 1, wherein the substrate comprises a silicon substrate.

3. (Previously Presented) The method of claim 2, wherein forming the oxide layer over at least a portion of the substrate comprises thermally growing an oxide layer.

4. (Previously Presented) The method of claim 1, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

5. (Previously Presented) The method of claim 4, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run in a range of approximately 1 second to approximately 30 seconds at a temperature of between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

6. (Previously Presented) The method of claim 1, wherein forming the oxide layer over the at least a portion of the substrate comprises forming an oxide layer having a thickness of about 30 Angstroms to about 50 Angstroms.

7. (Previously Presented) The method of claim 1, wherein patterning the resist to create the at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

8. (Currently Amended) A method for fabricating an integrated circuit device including N-channel and P-channel devices having selectively hardened gate oxides on a substrate, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

creating at least one hardened area within the oxide layer and at least one nonhardened area within the oxide layer <u>at a temperature approximately less than 90°C</u>;

stripping the first resist;

growing at least a portion of the at least one nonhardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

creating at least one second hardened area and at least one second nonhardened area within the at least one thick area of the oxide layer.

9. (Previously Presented) The method of claim 8, wherein the substrate comprises a silicon substrate and forming the oxide layer over the at least a portion of the substrate comprises thermally growing the oxide layer from the silicon substrate.

10. (Previously Presented) The method of claim 8, wherein creating the at least one hardened area within the oxide layer and the at least one nonhardened area within the oxide layer comprises conducting a high-density plasma remote plasma nitrogen treatment.

11. (Previously Presented) The method of claim 10, wherein conducting the high-density plasma remote plasma nitrogen treatment comprises conducting a process run for approximately 1 second to approximately 10 seconds at between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

12. (Previously Presented) The method of claim 10, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about30 Angstroms to about 50 Angstroms and growing at least a portion of the at least one nonhardened area within the oxide layer using the thermal oxidation process to form the at least one thick area within the oxide layer comprises growing at least a portion of the at least one nonhardened area to a thickness of about 50 Angstroms to about 70 Angstroms.

13. (Previously Presented) The method of claim 8, further comprising processing the substrate and the oxide layer to produce an integrated circuit device including at least one P-channel device including a hardened gate oxide and at least one N-channel device including a nonhardened gate oxide.

14. (Currently Amended) A method for fabricating an integrated circuit device including N-channel and P-channel devices on a substrate, each N-channel and P-channel device having selectively hardened gate oxides, the method comprising:
forming an oxide layer over at least a portion of the substrate;
forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

creating at least one hardened area within the oxide layer and at least one nonhardened area within the oxide layer at a temperature approximately less than 90°C;

stripping the first resist;

growing at least a portion of the at least one nonhardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

creating at least one second hardened area and at least one second nonhardened area within the at least one thick area of the oxide layer.

15. (Currently Amended) A method for fabricating a dynamic random access memory device on a substrate comprising:

supplying a substrate having an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer;

hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment having a temperature approximately less than 90°C;

processing the substrate and the oxide layer to create at least one P-channel device having a hardened oxide and an array of N-channel devices, each of the N-channel devices included within the array having a nonhardened gate oxide;

forming a second resist over at least a portion within the oxide layer;

patterning the second resist to create at least one second exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area and at least one second nonhardened area within the oxide layer.

16. (Previously Presented) The method of claim 15, wherein the substrate comprises a silicon substrate and forming the oxide layer over the substrate comprises growing an oxide layer from the silicon substrate.

17. (Original) The method of claim 15, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

18. (Original) The method of claim 17, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run for approximately 1 second to approximately 30 seconds at between about 30° C and about 90° C using about 800 watts to about 3000 watts of power.

19. (Previously Presented) The method of claim 15, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30 Angstroms to about 50 Angstroms.

20. (Previously Presented) The method of claim 15, wherein patterning the resist to create the at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

21. (Currently Amended) A method for hardening at least a portion of a gate oxide layer on a substrate, the method comprising:
forming an oxide layer over at least a portion of the substrate;
forming a resist over at least a portion of the oxide layer;
patterning the resist to create at least one exposed area of the oxide layer;
hardening the at least one exposed area of the oxide layer forming a hardened oxide layer having a first thickness and at least one nonhardened area within the oxide layer <u>at a temperature approximately less than 90°C</u>;
forming a second resist over at least a portion of the oxide layer;
patterning the second resist to create at least one second exposed area of the oxide layer; and
hardening the at least one second exposed area of the oxide layer.

22. (Original) The method of claim 21, wherein the substrate comprises a silicon substrate.

23. (Previously Presented) The method of claim 22, wherein forming the oxide layer over at least a portion of the substrate comprises thermally growing an oxide layer.

24. (Original) The method of claim 21, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

25. (Previously Presented) The method of claim 24, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run in a range of approximately 1 second to approximately 30 seconds at a temperature of between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

26. (Previously Presented) The method of claim 21, wherein forming the oxide layer over the at least a portion of the substrate comprises forming an oxide layer having a thickness of about 30 Angstroms to about 50 Angstroms.

27. (Previously Presented) The method of claim 21, wherein patterning the resist to create the at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.

28. (Currently Amended) A method for fabricating an integrated circuit device including N-channel and P-channel devices having selectively hardened gate oxides on a substrate, the method comprising:
forming an oxide layer over at least a portion of the substrate;
forming a first resist over at least a portion of the oxide layer;
patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

creating at least one hardened area within the oxide layer having a first thickness and at least one nonhardened area having a first thickness within the oxide layer at a temperature approximately less than 90°C;

stripping the first resist;

growing at least a portion of the at least one nonhardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

creating at least one second hardened area having another thickness and at least one second nonhardened area within the at least one thick area of the oxide layer.

29. (Previously Presented) The method of claim 28, wherein the substrate comprises a silicon substrate and forming the oxide layer over the at least a portion of the substrate comprises thermally growing the oxide layer from the silicon substrate.

30. (Previously Presented) The method of claim 28, wherein creating the at least one hardened area within the oxide layer and the at least one nonhardened area within the oxide layer comprises conducting a high-density plasma remote plasma nitrogen treatment.

31. (Previously Presented) The method of claim 30, wherein conducting the high-density plasma remote plasma nitrogen treatment comprises conducting a process run for approximately 1 second to approximately 10 seconds at between about 30° C and about 90° C using about 800 watts to 3000 watts of power.

32. (Previously Presented) The method of claim 28, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30 Angstroms to about 50 Angstroms and growing at least a portion of the at least one nonhardened area within the oxide layer using the thermal oxidation process to form the at least one thick area within the oxide layer comprises growing at least a portion of the at least one nonhardened area to a thickness of about 50 Angstroms to about 70 Angstroms.

33. (Previously Presented) The method of claim 28, further comprising processing the substrate and the oxide layer to produce an integrated circuit device including at least one P-channel device including a hardened gate oxide and at least one N-channel device including a nonhardened gate oxide.

34. (Currently Amended) A method for fabricating an integrated circuit device including N-channel and P-channel devices on a substrate, each N-channel and P-channel device having selectively hardened gate oxides, the method comprising:

forming an oxide layer over at least a portion of the substrate;

forming a first resist over at least a portion of the oxide layer;

patterning the first resist to create at least one exposed area of the oxide layer and at least one covered area of the oxide layer;

conducting a nitrogen hardening treatment <u>having a temperature approximately less than 90°C</u> to create at least one hardened area within the oxide layer having a first thickness and at least one nonhardened area within the oxide layer;

stripping the first resist;

growing at least a portion of the at least one nonhardened area within the oxide layer using a thermal oxidation process to form at least one thick area within the oxide layer having a second thickness;

forming a second resist over at least a portion of the at least one thick area within the oxide layer;

patterning the second resist to create at least one exposed area of the at least one thick area; and

conducting a second nitrogen hardening treatment to create at least one second hardened area and at least one second nonhardened area within the at least one thick area of the oxide layer.

35. (Currently Amended) A method for fabricating a dynamic random access memory device on a substrate comprising:

forming an oxide layer over at least a portion of the substrate;

forming a resist over at least a portion of the oxide layer;

patterning the resist to create at least one exposed area of the oxide layer having a first thickness;

hardening the at least one exposed area of the oxide layer using a remote plasma nitrogen hardening treatment <u>having a temperature approximately less than 90°C</u>;

processing the substrate and the oxide layer to create at least one P-channel device having a hardened oxide and an array of N-channel devices, each of the N-channel devices included within the array having a nonhardened gate oxide;

forming a second resist over at least a portion within the oxide layer;

patterning the second resist to create at least one second exposed area of the oxide layer; and

conducting a second remote plasma nitrogen hardening treatment to create at least one second hardened area having a second thickness and at least one nonhardened area within the oxide layer.

36. (Previously Presented) The method of claim 35, wherein the substrate comprises a silicon substrate and forming the oxide layer over the substrate comprises growing an oxide layer from the silicon substrate.

37. (Original) The method of claim 35, wherein hardening the at least one exposed area of the oxide layer using the remote plasma nitrogen hardening treatment comprises using a high-density plasma remote plasma nitrogen hardening treatment.

38. (Original) The method of claim 37, wherein using the high-density plasma remote plasma nitrogen hardening treatment comprises using a process run for approximately 1 second to approximately 30 seconds at between about 30° C and about 90° C using about 800 watts to about 3000 watts of power.

39. (Previously Presented) The method of claim 35, wherein forming the oxide layer over the substrate comprises forming an oxide layer having a thickness of about 30 Angstroms to about 50 Angstroms.

40. (Previously Presented) The method of claim 35, wherein patterning the resist to create the at least one exposed area of the oxide layer comprises patterning the resist to create a plurality of exposed areas of the oxide layer.